REMARKS

The Examiner's final Action mailed January 6, 2003, has been received and its contents carefully considered.

Claims 1-23 are pending in this application. The Examiner's allowance of claims 15-22, as indicated in Section 17 of the Action, is noted with appreciation. It is presumed that the inconsistent note on the Office Action Summary sheet, to the effect that all of claims 1-23 stand rejected, is an unintentional misstatement.

The Examiner has rejected claims 1, 3-7, 11 and 23 as being anticipated by Anzai (U.S. Patent No. 6,323,551). The rejection is respectfully traversed.

With regard to claim 1, the Examiner points to Anzai as disclosing a semiconductor apparatus comprising a semiconductor device (11d) to be mounted on a circuit board, a plurality of conductive posts ("leads", 13) electrically connected to the semiconductor device, and means for mounting the device onto a circuit board (col. 2, line 1) by soldering (via solder contacts, 16), including a plurality of conducting bumps (16) respectively positioned on an outer end of each of the conductive posts for soldering onto the circuit board, wherein a peripheral edge of a resin (15) covering for sealing a surface of the semiconductor and an outer edge of the conductive posts (exposed surface) are inherently separated by distances narrower than a height at the conductive posts.

As a general rule, terms in a claim should be interpreted in accordance with the disclosure. Anzai discloses conductive "leads" (16) which extend outward in a direction parallel to the surface of the semiconductor device (see Anzai Figure 1B), and not the "posts" claimed in the present application, which extend vertically from the semiconductor surface (see, for example, Application Figure 3). Contrary to the

Examiner's position, it is respectfully submitted that the leads of Anzai and the posts of the present invention are not equivalent.

Further, claim 1 recites the limitation " wherein a peripheral edge of a resin covering for sealing a surface of the semiconductor device and an outer edge of the conductive post are separated by a distance narrower than a height of the conductive post." It is respectfully submitted that Anzai fails to disclose this feature at all. What Anzai shows, in figure 1B for example, is that the resin covering (15) on the surface of the semiconductor device is limited to the space between the solder bumps, and is not close to the outer edge of the conductive post at all, much less separated by a distance narrower than a height of the conductive post, as claim 1 requires.

With regard to claim 7, the Examiner points to Anzai as further disclosing that the molded shape is to have a step (shown Figure 1A; via top molding, 15) along the entirety of a periphery edge of the semiconductor device, the step having upper (top surface) and lower portions (portion below solder, 16).

It is respectfully submitted that the Examiner is misapplying the teaching of Anzai. What is shown in Figure 1B of Anzai are two portions of the molding resin (15), an upper portion covering the device main surface, and a lower portion around the periphery of the device. Claim 7 specifically requires "a molding resin covering said device main surface, wherein said molding resin includes a step along the entirety of a peripheral portion of said device main portion, the step covering said post inner end portions, while leaving exposed said post outer end portions. It is respectfully submitted that the upper portion of the resin covering (15) shown in

Anzai Figure 1B has no step in it along the periphery of the semiconductor device. Rather, the resin covering simply ends at the solder balls

With regard to claim 11, the Examiner points to Anzai as further disclosing that the molding resin does not cover a peripheral side surface of each conductive post (Abstract), and an inherent insulating layer (via chip manufacture) formed on a peripheral surface of the semiconductor device between an upper surface of the semiconductor device and the conductive posts, wherein the molding resin is shaped to have a peripheral side surface on the identical plane with the side surface of the semiconductor device.

As noted above with respect to claim 7, the upper portion of the molding resin (15) that covers the surface of the semiconductor device in Anzai, ends at the inner side of the solder bumps, and hence, does not "have a peripheral side surface on the identical plane with the side surface of the semiconductor device," as claim 11 would require.

For at least the foregoing reasons, it is respectfully submitted that independent claims 1, 7 and 11, as well as their dependencies, claims 2-6, 8-14 and 23, patentably distinguish over the Anzai reference.

Without prejudice to the traversal herein of the prior art rejection based on Anzai, claim 1 is amended herein to recite the limitation "said resin covering leaving exposed said device peripheral side surface," thereby more clearly distinguishing over the Anzai reference. In Anzai, Figure 1B, the lower portion of the molding resin (15) is shown as being on the peripheral surface of the device. Similar changes are made to claims 7 and 11.

The Examiner has rejected claim 13 as being obvious over Anzai as applied to claim 11 and further in combination with Taguchi (U.S. Patent No. 6,285,085). The rejection is respectfully traversed.

Claim 13 depends from claim 11 and Taguchi fails to teach the features of the invention of claim 11 that the Examiner acknowledges are not disclosed by Anzai, namely, a second conductive bump formed on the respective peripheral portion of the conductive post. Therefore, it is respectfully submitted that claim 13 is patentable for at least the reasons advanced as to the patentability of claim 11. Moreover, according to Taguchi, a semiconductor device is not resin-molded. Taguchi illustrates in Figs. 1 and 13, a semiconductor device 12 having a step portion and bumps 22 and 23 formed to extend onto the step portion through an insulating layer 16. However, the insulating layer is not arranged in a groove formed at peripheral portion of the semiconductor device. Moreover, the bumps 22 and 23 extend into the groove. For that reason the teachings of Taguchi, make it difficult to prevent a short circuit generated between a bump and a semiconductor device. For these reasons, it is respectfully submitted that claim 13 is patentable the applied combination of Anzai and Taguchi.

The Examiner has rejected claims 1-10 under 35 USC 103(a) as being obvious over Yasunaga et al. (U.S. Patent No. 6,191,493). The rejection is respectfully traversed.

Claim 1, as amended, is directed to a semiconductor apparatus, which includes a semiconductor device, a plurality of conductive posts electrically connected to the semiconductor device, and means for mounting the device onto a circuit board by soldering, including a plurality of conductive bumps respectively

positioned on an outer end of each of the conductive posts for soldering onto the circuit board, wherein a peripheral edge of a resin covering for sealing a surface of the semiconductor device and an outer edge of the conductive post are separated by a distance narrower than a height of the conductive post.

Thus, according to a feature of the invention described in Claim 1, a distance ("d" in Figs. 3-8) between a peripheral edge of a molding resin and an upper edge of a conductive post is narrower or smaller than a height of the conductive post. Therefore, the connecting or bonding conditions of the bumps can be recognized visually during a mounting process. Further, the bumps are arranged adjacent the peripheral edge of the molding resin. This serves to improve an ability of the apparatus to radiate away heat.

Such a semiconductor apparatus is neither shown nor suggested by Yasunaga. See, for example, Fig. 81 of Yasunaga, which clearly shows the distance between the peripheral side surface of the molding resin 1 to be greater, in fact multiple times greater, than the height of the conductive post 9. Therefore, the Yasunaga apparatus cannot provide the above described advantages of the invention that the connecting or bonding conditions of the bumps can be recognized visually during a mounting process and so substantially improve an ability of the apparatus to radiate heat away.

Accordingly, it is respectfully submitted that claim 1, as well as claims 2-6 depending therefrom, patentably distinguish over Yasunaga.

Claim 7 is directed to a semiconductor apparatus, which includes a semiconductor device, a plurality of conductive posts electrically connected to the semiconductor device, means for mounting the device onto a circuit board by

soldering, including a plurality of conductive bumps respectively positioned on an outer end of each of the conductive posts for soldering onto the circuit board, and a molding resin covering a surface of the semiconductor device, wherein the molding resin is shaped to have a step along the entirety of a peripheral edge of the semiconductor device, the step having upper and lower level portions. As a result, connecting or bonding conditions of bumps can be visually recognized in a mounting process. Further, a bonding area between a conductive post and a bump is increased, so that reliability of such bonding is increased.

Such a semiconductor apparatus is neither shown nor suggested by Yasunaga. For example, see again Fig. 81 of Yasunaga, which clearly shows no evidence of a step along the entirety of a peripheral edge of the semiconductor device, the step having upper and lower level portions. Therefore, the Yasunaga apparatus cannot provide the above-described advantages of the invention that the connecting or bonding conditions of the bumps can be recognized visually during a mounting process.

Accordingly, it is respectfully submitted that claim 7, as well as claims 8-10 depending therefrom, are patentable over Yasunaga.

Based on the above, it is submitted that this Amendment places the application in condition for allowance and accordingly, should be entered pursuant to 37 CFR §1.116. Notice of allowance, with allowed claims 1-23, is earnestly solicited.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

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Date

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